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FOR

A METHOD AND APPARATUS FOR BATTERY POWER PRE-CHECK AT
SYSTEM POWER-ON

Inventor:

Don Nguyen

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Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025-1030
(408) 720-8598

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A METHOD AND APPARATUS FOR BATTERY POWER PRE-CHECK AT SYSTEM POWER-ON

CROSS REFERENCES TO RELATED APPLICATIONS

This is a continuation of application Ser. No. 09/162,643, filed September 29, 1998, currently pending.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to the field of portable computing devices. More particularly, the present invention relates to testing batteries to determine whether power should be supplied to particular components when an attempt is made to fully or partially enable or otherwise increase the power consumption of the system.

2. Description of Related Art

Many portable computing or other electronic devices are powered by batteries. Inevitably, unless charged, such batteries discharge and are no longer able to maintain operation of their host device. Users, however, often attempt to turn on their portable electronic devices either because they are unaware of the fact that the batteries are discharged or in an attempt to obtain additional operation from the failing batteries.

Unfortunately, failing batteries may cause problems for some electronic devices. For example, some electronic devices contain components which do not function properly when insufficient power is supplied. As a result, certain operations may be performed

inaccurately and/or data may be corrupted. Even worse, other components may be damaged when insufficient battery power is available.

In general, some prior art devices detect and react to low battery power. In particular, prior art portable computer systems often utilize hardware such as a System Management Controller (SMC) which communicates with various system batteries and components over a System Management Bus (SMBus) to manage power consumption. Further details regarding the SMBus protocol are available in the SMBus Specification, Revision 1.0, February 15, 1995, available from the Smart Battery System Implementer's Forum (on the Internet at the time of filing of this application at www.sbs-forum.org).

Prior art computer systems typically only monitor batteries during normal operation. Such systems use the SMBus or other power control hardware in warning the user of low battery power and/or shutting down the system if needed. Additionally, some systems switch between primary and secondary battery supplies during normal operation and even temporarily resort to using a back-up battery to shut down the system in an orderly fashion to avoid the loss of data.

The prior art does not, however, provide a technique which performs a pre-check of battery levels. That is, the prior art does not test power levels of the batteries which would otherwise supply power to electronic components before such batteries are allowed to power such electronic components. Consequently, it would be possible for an improperly charged (i.e., overcharged or undercharged) battery to damage such components.

Brief Description of the Figures

The present invention is illustrated by way of example and not limitation in the Figures of the accompanying drawings.

Figure 1 illustrates one embodiment of a system utilizing a battery power pre-check circuit.

Figure 2 illustrates one embodiment of a method for determining whether to provide power to system components using a battery check circuit.

Figure 3 illustrates one embodiment of a computer system which includes a battery check circuit which may determine whether either a primary battery or a secondary battery has sufficient power for the computer system.

Figure 4 illustrates details of one embodiment of the battery check circuit which may be used in the computer system illustrated in Figure 4.

Figure 5 illustrates one embodiment of a process performed at system power-on for a system such as one utilizing components in Figures 3 and 4.

Detailed Description

The following description provides a method and apparatus for battery power pre-check at system power-on. In the following description, numerous specific details such as types of portable electronic devices, battery test logic implementation, and logic partitioning/integration choices are set forth in order to provide a more thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the invention may be practiced without such specific details. In other instances, control structures and gate level circuits have not been shown in detail in order not to obscure the invention. Those of ordinary skill in the art, with the included descriptions, will be able to implement the necessary logic circuits without undue experimentation.

The disclosed apparatus and method may advantageously protect components or data in a portable computer system or other battery powered electronic device. This protection involves the use of a battery check circuit which determines whether power from a battery should be applied to one or more components by testing a power level of the battery. In some embodiments, a back-up battery may be used to temporarily power the battery check circuit and/or system components while the test is performed. The battery check circuit may prevent power from being supplied to other components and shut down the battery check circuit itself if insufficient power is available to adequately power the system.

Figure 1 illustrates one embodiment of a system utilizing a battery check circuit 100. The system may be a laptop or notebook computer, a personal digital assistant, as well as any other type of portable electronic component which is capable of operating on battery power. The illustrated system includes a processor 140, a memory 150, and input/output (I/O) device(s) 160. The processor 140, the memory 150, and the I/O devices 160 receive power via one or more power supply line(s) 137, and transfer information over a bus 145. Many other types and/or combinations of components may be used in a system in combination with the battery check circuit 100.

The battery check circuit is coupled to an on/off switch 110. In a laptop computer this may be a push-button switch which, when temporarily depressed, indicates that the user wishes to power-on the system. In other embodiments, the power-on may be accomplished by other sensing or mechanical mechanisms. For example, opening the lid of a portable device may be used to signal that the device should be enabled. Alternatively, writing on a touch-pad or moving a mouse, or many other types of stimulus could be received by the battery check circuit 100 to signal system power-on.

A sequence of operations which may commence with system power-on is illustrated in Figure 2. This sequence of operations may be used in some embodiments at times other than power-on when a change in the power consumption level of the system changes. For example, such a sequence may be employed when the system is awakened from a low power state or at other times when a significant change in power consumption is about to occur.

As illustrated in Figure 1, a battery 120 is connected to a power supply line 125 to the battery check circuit 100. As indicated by step 205, the battery check circuit typically

needs power to perform the battery check. In some embodiments, the battery check circuit 100 is powered by a back-up battery (not shown); however, in other embodiments the battery check circuit may be able to receive sufficient power from the battery 120.

As illustrated in step 210, the battery check circuit tests the primary battery or batteries. In the case of Figure 1, the battery 120 is tested. The battery check circuit 100 may perform a variety of checks on the battery 120. For example, the battery check circuit 100 may determine whether the battery 120 has sufficient power to supply the processor 140 and other components with the proper voltage and/or current level.

Alternatively, the battery check circuit 100 may perform tests to make sure that the battery 120 will not supply too high of a voltage for the components. In general, the battery check circuit may perform any of a variety of tests which may determine whether the battery 120 may be safely applied to the components without jeopardizing either the components themselves, operation of other components, or any information stored in the system. If the battery 120 fails the test performed by the battery check circuit 100 in step 215, the battery check circuit 100 has determined that there is an unacceptably high risk of malfunction or damage and therefore the battery check circuit 100 does not connect the battery 120 to the system as shown in step 220.

If the battery check circuit 100 determines that sufficient power is available to safely operate the system in step 215, the switch 135 is closed and the battery is connected to power supply line(s) 137 enabling the main power supply as shown in step 225. Typically, the switch 135 is an electrically actuated switch. In addition to the switch 135, there may be a direct current (DC) to DC converter, a voltage regulator, or other circuitry which is enabled by the power check circuit 100 (as part of the process of

enabling the main power supply) to ensure an appropriate supply voltage to the processor 140 and other components.

In some embodiments, the battery 120 itself generates an appropriate voltage for the components, and there may be no need for extensive power regulation and conversion devices, thereby making the role of the battery power check circuit 100 even more important for protecting the components. In such cases, the main power supply may be enabled simply by closing the switch 135 to supply power to the system components, although some form of power filtering (active or passive) will typically be employed as well.

After the main power supply is enabled and the components receive power, the battery check circuit 100 may be disabled as shown in step 230. This step, however, is an optional way to save power. Instead, the battery check circuit 100 may be left on or may play an active role as the system transitions between various power levels.

Figures 3 and 4 illustrate details of one embodiment of a portable computer system which utilizes a battery check circuit 300 at system power-on. In Figure 3, the top level system schematic is shown, whereas Figure 4 illustrates additional details of one embodiment of the battery check circuit 300 and associated components. Figure 5 illustrates an associated sequence of operations for one embodiment.

The system of Figure 3 includes various computer system components as well as the battery check circuit 300. The battery check circuit 300 is powered either by a back-up battery 305 via a supply line 307 or by power from an alternating current (AC) adapter input provided on a supply line 310. If power is available from the AC adapter input, it may not be necessary to check the status of the power from system batteries. For the

remainder of the discussion of this embodiment, unless otherwise specified, it is assumed that power is not available from the AC adapter input.

The components illustrated in Figure 3 include a processor 370, a memory 375, a north bridge 380, a south bridge 385, and I/O device(s) 390. The processor 370, memory 375, and north bridge 380 communicate via a host bus 372, and all of these components are powered by Vcc1 on a supply line 367. The south bridge 385 is coupled to the north bridge 380 via a secondary bus 382, to a control bus 335, and to the I/O device(s) 390 by a bus 387. The south bridge 385 and the I/O device(s) 390 are shown as being powered by a second voltage supply line 369 (Vcc2). This configuration is only an exemplary arrangement in which the presently disclosed techniques may be used. Many other arrangements of components (or even a single component) may benefit from the use of battery check circuitry.

When the on/off switch 110 is depressed, a power latch 320 senses a momentary impulse from the on/off switch 110 as indicated in step 505 of Figure 5. The power latch 320 latches a value such that power from the back-up battery 305 (and/or the primary battery 340 and the secondary battery 350 if sufficiently charged) is provided on a start-up supply line 322 as indicated in step 510. A start-up circuit 325 receives power via the start-up supply line 322 and provides a back-up supply voltage on supply line 327.

A PWRGOOD signal on a signal line 366 controls a switch 328 and initially opens the switch 328, thereby only providing the back-up supply voltage to the battery check circuit 100 during system startup. The entire system typically first receives power when its main supply is enabled.

Step 510 also indicates that in one embodiment the latch may operate by utilizing a resistive-capacitive (RC) timing circuit to assert a preset input. This technique is used in the embodiment of the battery check circuit shown in Figure 4. In the embodiment of Figure 4, either AC adapter power on a supply line 402, DC power from the primary or secondary battery (not shown), or a back-up battery 408 may supply power during this initial start-up phase. When external AC power is available, that power not only supplies power for the system, but also recharges the back-up battery via a battery charger 406.

An AC-NOT-PRESENT signal 490 (when asserted low) indicates that AC adapter power on the supply line 402 is present with sufficient voltage. In conjunction with a diode 491, the AC-NOT-PRESENT signal therefore turns off the N channel transistor 476 by producing a low value at its gate. Node 419 is pulled up approaching the voltage on node 416. The diode 426 is forward biased providing a high logic level at the gate of N channel transistor 482. With transistor 482 turned on, the P channel transistor 424 is enabled, and power is supplied to the start-up regulator 430 which generates Vccbk at that time.

The back-up battery 408 is coupled via a supply line 409 and a diode 412 to a node 416. The AC adapter power is similarly coupled to node 416 via the supply line 402 and a protection diode 410. Although not shown in Figure 4, the primary battery and the secondary battery are similarly coupled by diodes to provide power at node 416. Thus, node 416 receives power at any time that any power source is available. Since the backup battery 408 usually has a lower voltage than the primary battery and the secondary battery, the backup battery 408 will usually not be discharged due to the diode arrangement. When an on/off switch 484 is depressed, a connection is made between

node 416 and ground through a resistor 420 which is connected between node 416 and node 421.

A P-channel transistor 424 having a source connected to node 416, a drain connected to a V_{in} terminal of a start-up regulator 430, and a gate connected to node 421. Due to the closing of the switch 484, the transistor 424 begins conducting due to the voltage drop across the resistor 420. Accordingly, the start-up regulator 430 receives the voltage supplied at node 416 and produces a voltage V_{ccbk} at its output V_{out} which is connected to a supply line 432. Thus, even if the primary battery or batteries have insufficient power, the battery check circuit and the V_{ccbk} rail are powered by the backup battery.

The V_{ccbk} power supply is provided at the data (D) and clock (CLK) inputs of a latch 444. V_{ccbk} is also provided to the preset input of the latch 444 through an RC circuit formed by a capacitor 440 and a resistor 438. The RC circuit keeps the preset input asserted as power ramps on supply line 432, thereby ensuring that the latch output (Q) is set to drive a logical one on node 478. The logical one on node 478 enables an N-channel transistor 482 which provides a connection from node 416 to ground through the resistor 420. Accordingly, when the switch 484 is released, the enabled transistor 482 keeps the gate of the transistor 424 at a low voltage level such that power from the back-up battery is latched as indicated in step 510.

Referring back to Figure 3, after the power supply for the battery check circuit 300 is latched, a battery test circuit 330 sends signals over the control bus 335 effectuating a test of a primary battery 340 and/or the secondary battery 350 as indicated in step 520. In one embodiment, the battery test circuit 330 may be a part of a system management

controller (SMC) and the control bus may be a System Management Bus (SMBus) which operates in accordance with the SMBus Specification mentioned in the background section of this disclosure. In this embodiment, the primary battery 340 and the secondary battery 350 are “smart batteries” which are capable of receiving and responding to commands such as power level testing commands over the control bus 335. Additionally, the SMC itself may be powered by the back-up battery via the power supply line 432 (Vccbk) as shown in Figure 4. Alternatively, other types of control interconnections and signaling conventions may be used for communications with and testing of the batteries and the battery check circuit.

A voltage or power level value is returned to the battery test circuit 330 from one or both of the primary battery 340 and the secondary battery 350 and compared to a predetermined value to determine if the batteries have sufficient power to run the system at the new power level as indicated in step 525. Alternatively, other tests or comparisons may be performed which detect whether the tested battery can power the system without causing malfunction or damage.

If insufficient power is available from both the primary battery 340 and the secondary battery 350, the battery check circuit 300 does not power up the system as indicated in step 530. Referring to the detailed schematic of Figure 4, in response to the insufficient power being available, the SMC 330 asserts a START-UP SHUTDOWN signal on a signal line 460 as shown in step 535. The START-UP SHUTDOWN signal is connected to the gate of an N-channel transistor 448 and connects a clear input of the latch 444 to ground in response to the assertion of the START-UP SHUTDOWN signal, thereby resetting the latch 444 to zero.

In response to the logical zero on node 478, the transistor 482 is disabled, resulting in the transistor 424 being shut off. Consequently, the back-up battery 408 and all other battery power is disconnected from the start-up regulator 430 and the POWERGOOD signal will not be asserted to close the switch 328. In Figure 3, the battery check circuit 300 does not assert an ENABLE REGULATOR signal on the signal line 329. Thus, the detection of insufficient battery power prevents the entire system from operating and prevents power from the primary and secondary batteries from being provided to any system components. Finally, the back-up battery may be disconnected from the battery check circuit 300 and any other system components as indicated in step 540.

If either battery has sufficient power for the system, the battery check circuit 300 may assert the ENABLE REGULATOR signal on a signal line 329 as indicated in step 545. The battery check circuit 300 may also pass commands indicating which battery to select to an input power select circuit 360. The input power select circuit 360 is coupled to select, as a supply voltage for a voltage regulator 365, one of the primary battery output voltage (Vbp) on a supply line 342, the secondary battery output voltage (Vbs) on a supply line 352, and the AC adapter input on the supply line 310. In response, the input power select circuit 360 provides power from the appropriate source to the regulator via a supply line 362.

When the regulator 365 achieves stable supply voltages Vcc1 on the supply line 367 and Vcc2 on a supply line 369, the PWRGOOD signal is driven on signal line 366 as shown in step 550. Referring to Figure 4, assertion (to a logical high value) of the PWRGOOD signal closes the switch 328 rapidly and more slowly resets the latch 444

such that the switch 328 is closed before power to the startup regulator is disabled by turning off transistor 424.

To achieve the proper sequencing, a resistor 454 and a capacitor 452 are connected to form an RC circuit which provides a delay before a gate input of an N-channel transistor 446 reaches a logical high level. The logical high level at the gate of the transistor 446 enables that transistor, and clears the latch 444 as indicated in step 555. As previously, resetting the latch disconnects the back-up battery from the start-up circuit 430 as indicated in step 540. Vccbk remains powered by the Vcc1 rail through the closed switch 328 so that the SMC 330 may continue to operate without draining the backup battery 408.

Additionally, when the PWRGOOD signal is asserted, it passes through a diode 470 to node 474. The PWRGOOD signal asserted (logical high value) enables an N-channel transistor 476. Accordingly, transistor 482 turns off, and power may not continue to pass through transistor 424. Thus, the back-up supply node 416 is disconnected from the battery check circuit 300 and normal operation commences.

A method and apparatus for battery power pre-check at system power-on has been disclosed. While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art upon studying this disclosure.